ARG 1834
User Manual

ISSUE 5

TITLE	DRAWN	CHECKED	APPROVED	DATE
ARG 1834 USER MANUAL	CRW	GF	CRW	20.4.98
	DRAWING NO: 1834-EQ001-PS1			

ISSUE	DESCRIPTION	APPD	DATE
3	ECN4156	MH	30.09.99
4	ECN4463	MH	10.01.01
5	ECN4479, ECN4514	SL	18.05.01

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Installation *PLEASE READ THIS SECTION CAREFULLY*

Both the ARG1834 TX and RX units are intended to be installed in standard 19" Euroracks in an indoor environment. To comply with IEC 950 safety requirements, **there should be adequate means nearby to isolate the units from the mains supply in an emergency**. As the units are Class 1 equipment, **a mains earth must be provided via the mains input socket**. An additional chassis bonding point is also provided on each unit. The units are **not** intended to be operated with any part of the casing removed. There are hazardous voltage accessible within the units. **For the 48 VDC powered version, it is strongly recommended that the chassis bonding stud is wired to local bonding, as the 48VDC supply input is isolated from the case.**

Warranty

These units are warranted against failure due to poor workmanship or defective materials for a period of 2 years from date of shipment. There are no user-serviceable parts inside - any servicing or other operations requiring access to the internal parts must be referred to qualified personnel, who must use full precautions to avoid the possibility of damage to the unit by static electricity or other means. Any evidence of unauthorised access to the internal parts will be regarded as invalidating this warranty. All external features, and in particular the connectors, should be kept free from damage or undue ingress of water, dirt, grease, solvents or other contaminants at all times.

Claims against this warranty will be treated on an individual basis, and will not be upheld if there are signs of accidental or intentional damage or mistreatment, or if the unit has been stored or operated outside its recommended temperature range.

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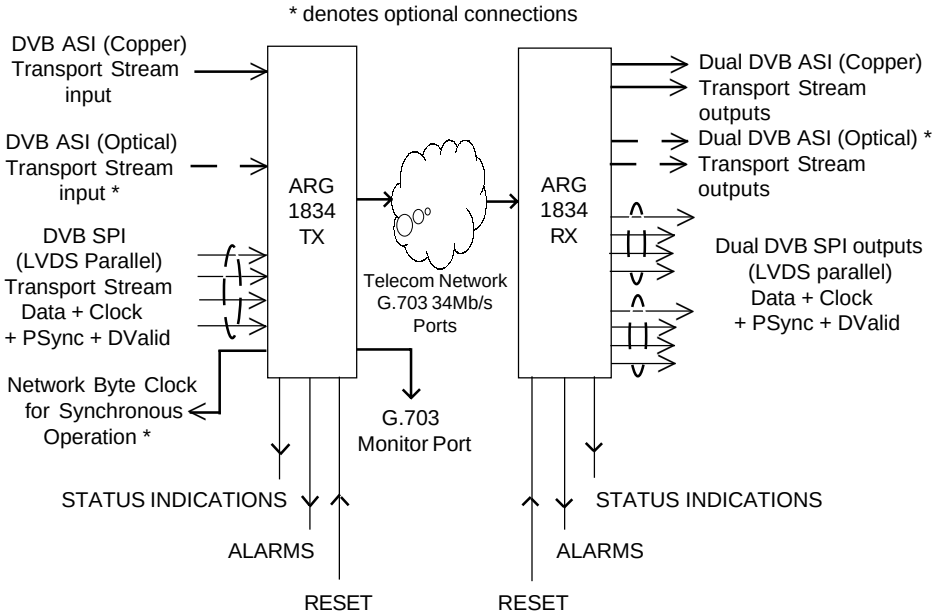
ARG1834 TX/RX USER MANUAL

INTRODUCTION

This document defines the features, connections and fundamental operating principles of the ARG1834 TX and RX Telecom Network Adaptor Units, the main function of which is to enable the transmission of MPEG-2 or other data streams over PDH or SDH telecoms networks using 34Mbs (E3) ports. The system design includes the capability of rate adaption, so that data streams operating at less than 34Mb/s can be modified, transported and subsequently recovered (also referred to as 'Fractional Bandwidth' availability). In addition, DVB-compliant Reed-Solomon forward error correction (204, 188; 8) is incorporated to control the integrity of the transmission over the Telecom Network. Convolutional interleaving, depth 12, is set as default.

Please note that data transmission is SIMPLEX (one way only), and that both (TX and RX) units are required to enable Telecom Network connection. A proprietary rate adaption algorithm has been adopted to minimise transmission 'overhead'.

ARG 1834 TX/RX BLOCK DIAGRAM


* denotes optional connections
DVB ASI (Copper) Transport Stream input
DVB ASI (Optical) Transport Stream input *
DVB SPI (LVDS Parallel) Transport Stream Data + Clock + PSync + DValid
Network Byte Clock for Synchronous Operation *
ARG 1834 TX
Telecom Network G.703 34Mb/s Ports
G.703 Monitor Port
ARG 1834 RX
Dual DVB ASI (Copper) Transport Stream outputs
Dual DVB ASI (Optical) * Transport Stream outputs
Dual DVB SPI outputs (LVDS parallel) Data + Clock + PSync + DValid
STATUS INDICATIONS
ALARMS
RESET
STATUS INDICATIONS
ALARMS
RESET

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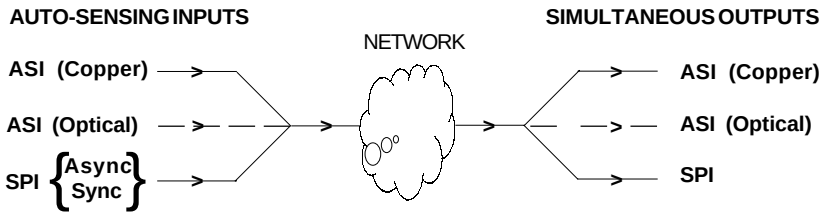
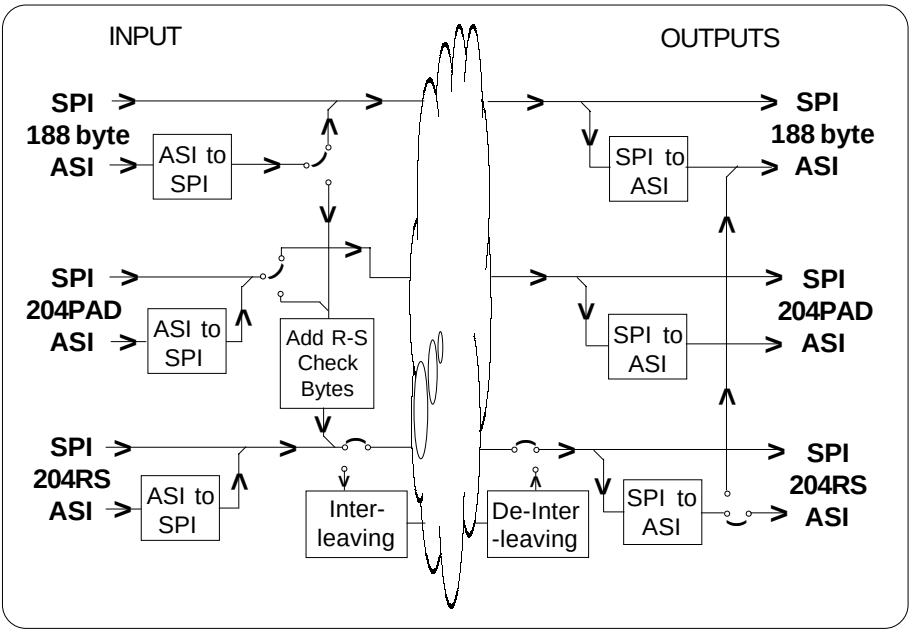
ARG1800 SERIES - ALLOWED CONVERSION OPERATIONS

1800 SERIES TRANSMITTER **1800 SERIES RECEIVER**

TRANSPORT STREAM PHYSICAL INTERFACE





Notes:

1. ASI outputs are byte spaced or packet spaced, whichever was originally input, by default.
2. ASI output spacing can be forced to byte or packet (not if also using 188 to 204 conversion.)
3. If the input is in SPI format, the ASI outputs will be packet spaced by default.
4. With the correct links, 188 byte packets can be automatically reconstructed at the Rx unit.

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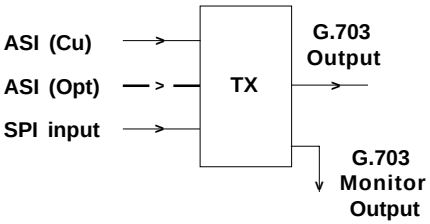
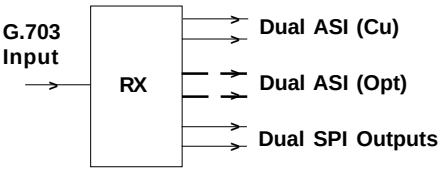
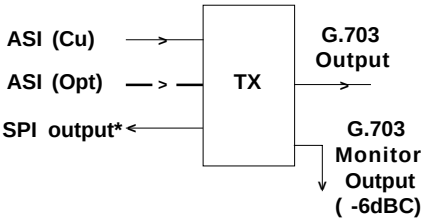
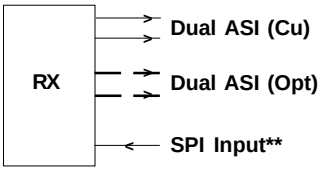
ARG1800 SERIES - MONITORING AND ASI/SPI CONVERSION FUNCTIONS









***SPI port can be used as a monitor output, or purely for ASI to SPI conversion.**

**** SPI port can be used as an input, for SPI to ASI conversion.**

Note: Optical ASI ports are a factory fit option, and are not fitted as standard.

OTHER OPTIONS

TRANSMITTER

- Mains/48 VDC Power Supply
- G.703 Cable shield earthing (usually earthed at TX end)
- Bit order inversion (for compatibility with other OEM G.703 streams).
- Reed-Solomon on/off
- Interleaving on/off
- Support for non-MPEG SPI data
- 188 byte to 204 RS conversion
- 204 PAD to 204 RS conversion

RECEIVER

- Mains/48 VDC Power Supply
- G.703 Cable shield earthing (usually isolated at RX end)
- Bit order inversion (for compatibility with other OEM G.703 streams).
- Reed-Solomon on/off
- De-Interleaving on/off
- Support for non-MPEG SPI data
- Alarm desensitisation (noisy lines)
- Forcing byte or packet space (ASI)
- 204 byte to 188 byte re-conversion
- G.703 line equalisation setting

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1.0 ARG1834 TX SPECIFICATION

The ARG1834 TX unit contains the necessary functionality to accept an MPEG-2 Transport Stream, in either DVB ASI (serial) or DVB SPI (parallel) form, or in fact any 8 bit parallel data + clock, perform parallel-to-serial conversion where necessary, rate adaption, Reed-Solomon error correction checking and re-encoding, byte Interleaving if required, monitor for fault or alarm conditions, and transmit the serial data stream so produced over a digital Telecommunications Network conforming to ITU-T Recommendation G.703, at a gross line rate of 34.368Mb/s (E3).

Input Interfaces	: Synchronous parallel DVB SPI interface (8 bit parallel data + clock); or :Asychronous serial DVB ASI interface (Copper standard - fibre-optic available as a factory option) as defined in EN 50083-9, and DVB-PI-232 (previously DVB-PI-154)
Input Data Rate	: In the range 8-32.2 Mb/s, or 34.368Mb/s synchronous
Input Connectors	:25 way 'D'-type female with threaded locking posts (SPI) or :75 ohm BNC coaxial (ASI Copper) or :SC type connector, multi-mode fibre (ASI Optical)
Input signal levels	: LVDS (Low Voltage Differential Signalling) (SPI) or :200-880mV into 75 ohms (ASI Copper) or :-26 to -14dBm (average) (ASI Optical)
MPEG Framing structure	:As defined in EN 50083-9 and DVB-PI-232, where framing applicable
Clock Output	: CLOCKA, CLOCKB @ 4.296MHz (Used in Synchronous mode)
Clock Output Connector	: 25 way female 'D' type with threaded locking posts
Clock o/p signal levels	: LVDS (Low Voltage Differential Signalling)
Telecom Output Interface	: ITU-T G.703 E3 interface at 34.368Mb/s using HDB-3 line coding
Frame Structure	: Proprietary
Output Level	: Compliant with ITU-T Recommendation G.703
Output Connector	: 75ohm BNC coaxial
G.703 Monitor Port	: BT type 43 connector, level nominally -6dB below main output
Power Supply	: Single-phase auto-sensing mains input, 100-240Vrms a.c., 50-60 Hz or : 48 VDC(factory option) 40.5-57VDC range Typical consumption : 20VA
Mains Input Fuse Rating	: 2AT (2 Amp Anti-Surge (T) as per IEC 127) and UL recognised.
48 VDC Input Fuse	: 2A quickblow
Auxiliary Control Signals	: Summary alarm / fail indications, via Form 'C' relay contacts, with reset input

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Auxiliary Connector	:9-way 'D'-type female with threaded locking posts
Operating Temperature	:0degC to +40degC
Storage Temperature	:-5degC to +70degC
Safety	:EN 60950 73/23/EEC (LVD Europe), UL 1950 3rd edition, CSA 950-95
EMC	:EN 55022 , EN 50082-1, 89/336/EEC (Europe) 47CFR CH.1 (FCC) Part 15, Subpart B, Class A
Link Options	**(Refer to sections 1.8 and 1.9 for link locations).** : FEC on/off (factory default = on) (see section 1.1.4) : Interleaving on/off (factory default = on) (see section 1.1.5) : Bit order inversion (see section 1.3.3) (for compatibility with certain OEM equipment) : 188 byte to 204RS MPEG packet conversion (see section 1.1.4) (i.e. addition of RS FEC) : 204PAD to 204RS MPEG packet conversion (2 links) (i.e. addtion of RS FEC) (see section 1.1.4) : Enable transport of 204PAD from an ASI source (see section 1.1.4) : Use of SPI port as an output (see section 1.1.6) (for monitoring, or for ASI to LVDS conversion) : Transmission of non-MPEG SPI data (see section 1.4.1/1.4.2) (not in Synchronous mode)
Factory options	: ASI Optical input, 48 VDC power i/p : Contact factory for T1, E1, E2, DS-3, E4, STM-1 variants

1.1 Input Interfaces

1.1.1 The LVDS parallel input accepts any suitable 8-bit parallel data with an accompanying byte clock. If the data rate is in the range 8-32.2 Mb/s, it will automatically be rate-adapted upwards for transmission over the E3 Telecom Network. Alternatively, the unit will also accept synchronous data at the Network net data rate of 34.368 Mb/s. See Section 1.1.6 for connector pin allocation details. A synchronising clock for the preceding equipment is provided at the Network **byte** rate (see section 1.2, Clock Output Interface).

1.1.2 The ASI serial inputs accept a serial data stream operating at 270Mb/s gross bit rate. Data rates in the range 8-32.2Mb/s will be automatically rate-adapted upwards for transmission over the E3 Network interface. **Data rates outside this range should not be used with the ASI inputs.**

1.1.3 The ARG 1834 TX unit will lock on to incoming transport streams from its inputs with the following priority:

<1> ASI Copper <2> ASI Optical <3> SPI (LVDS)

However, once locked, switching to another input will **not** occur unless the existing input signal is lost (loss of carrier or loss of MPEG frame lock). LEDs on the front panel report the activity/status of the inputs (see Section 1.6).

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1.1.4 The ARG 1834 TX unit automatically senses the incoming data rate and packet type and configures its operation accordingly. The incoming data may be from an MPEG-2 source, in which case the data is expected to be fully compliant with EN 50083-9 and DVB-PI-232, and the ARG1834 TX unit will accept, and automatically differentiate between, the following:

a) packets of 188 data bytes
b) packets of 188 data bytes plus 16 padding bytes (link needed if ASI input - see 1.8)
c) packets of 188 data bytes plus 16 Reed-Solomon check bytes

Link options are also available to allow the conversion of either 188 byte packets or 204 PAD packets into 204 RS packets, thereby adding forward error correction to protect the integrity of data over the telecom link. Interleaving is also available as a link option, factory default = on

Padding bytes are otherwise transmitted transparently **(note that an internal link is needed to transport 204 padded streams from an ASI source - see Section 1.8)**, whereas Reed-Solomon check bytes are used to correct received errors if possible. If the errors are not recoverable, the error flag bit in the packet header will be set to '1' and the data will be left unchanged. The Reed-Solomon check bytes will be recalculated to protect the 'new' data. The ARG1834 TX unit cannot reset the error flag bit if already set to '1' within the incoming data stream. If there are no errors detected, or if the received errors are recoverable, the recalculated Reed-Solomon check bytes will be forwarded on to protect the integrity of the data over the Telecoms Network.

Note: A link option is available to disable Reed-Solomon operation if desired (see section 1.9, link JP24).

1.1.5 DVB - compliant byte Interleaving (depth 12) is set as default to further protect the integrity of data transmission. (see section 1.9) Please note that an appropriate De-Interleaving operation will then be required at the receive end, which is fitted on as default.

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1.1.6 Connection to an incoming DVB SPI parallel data stream is made via a 25 way 'D' type female connector mounted on the rear panel, as follows:

Pin Connections (LVDS levels) :

Pin		Signal	Pin		Signal
1	:	ClockA input	14	:	ClockB input
2	:	System Gnd	15	:	System Gnd
3	:	Data 7 A (MSB)	16	:	Data 7 B (MSB)
4	:	Data 6 A	17	:	Data 6 B
5	:	Data 5 A	18	:	Data 5 B
6	:	Data 4 A	19	:	Data 4 B
7	:	Data 3 A	20	:	Data 3 B
8	:	Data 2 A	21	:	Data 2 B
9	:	Data 1 A	22	:	Data 1 B
10	:	Data 0 A	23	:	Data 0 B
11	:	DValid A	24	:	DValid B
12	:	PSync A	25	:	PSync B
13	:	Cable Shield			

Data should change on the falling edge of the clock on pin 1.

Notes:

a) The incoming data rate can be from 8-32.2 Mb/s (any input), or 34.368Mb/s (DVB SPI parallel input only) (see note b). If the incoming data rate is higher than that allowed, an Alarm/ Fail condition will be signalled.

b) 'Transparent' byte-wise 34.368Mb/s input data can be transported if synchronised to the Telecom Network using the clock provided on the Clock Output Interface Connector, as detailed in Section 1.2 ('Synchronous' mode). In this mode the ARG 1834 TX unit feeds a synchronising byte rate clock back to the preceding equipment, which the latter must then use to clock the data out to the ARG 1834 TX unit.

c) The SPI (LVDS) data port can be configured as an output, either for monitoring purposes or so the unit can act as an ASI to SPI convertor (see Section 1.8 for links)

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1.2 Clock Output Interface (Synchronous mode)

The ARG 1834 TX provides a clock output at the Telecom Network **byte** rate, 4.296Mbytes/ sec, for synchronising the preceding equipment to the line payload byte rate, if required. The clock signals are in

LVDS (Low Voltage Differential Signalling) form, and are available on the rear panel via a separate 25 way female 'D' type connector mounted on the rear panel, as follows:

Pin Connections: (All other pins not connected)

LVDS (Female 'D' Type)

Pin	**:**	**Signal**
Pin 1	:	ClockA
Pin 14	:	ClockB
Pin 13	:	0v (Cable shield)

1.3 Telecom Network Output Interface

1.3.1 The main Telecom Network output has been designed to comply with ITU-T Recommendation G.703 for Physical/Electrical characteristics of hierarchical digital interfaces at a bit rate of 34.368Mb/s. HDB-3 line coding is used, and a 75ohm BNC coaxial socket is provided on the rear panel. The Network connection is transformer-coupled.

1.3.2 A G.703 monitor output is also provided on the rear panel, via a BT type 43 coaxial connector, the outer of which is connected to signal ground. The output level, into 75 ohms, is nominally -6dB below the main G.703 output.

1.3.3 The order of bits transmitted to line can be inverted for compatibility with certain OEM products, (see section 1.9 for location of link.)

1.4 Auxiliary Interface

The ARG1834 Tx unit provides alarm/fail/reset functionality via a 9 way filtered 'D' type female connector on the rear panel.
The ARG1834 TX unit may be reset by the application of a short circuit between pins 5 and 9 on the Auxiliary Connector. While this condition is applied and held, the ARG 1834 TX unit will be held in a reset state in which it will not respond to data in the MPEG-2 Transport Stream. Both the Alarm and Fail relays will be de-activated, signalling an Alarm/Fail condition to appropriately connected equipment. Internally stored alarm/fail states, and any other internally stored status information, will be erased. Upon removal of the short circuit, the ARG1834 TX will go through a re-start sequence in which major circuit functions will be re-initialised. There will be a finite delay before the unit will re-commence data transmission over the Telecom Network.

Pin connections:

Pin		Signal
Pin 1	:	Protective ground
Pin 2	:	Fail relay (Common)
Pin 3	:	Alarm relay (Normally Open in Alarm condition)
Pin 4	:	Alarm relay (Normally Closed in Alarm condition)
Pin 5	:	Reset input 1
Pin 6	:	Fail relay (Normally Open in Fail condition)
Pin 7	:	Fail relay (Normally Closed In Fail condition)
Pin 8	:	Alarm relay (Common)
Pin 9	:	Reset input 2
Relay type	:	BT Type 53, Contact rating: 1A switch, 125V dc/ac, 30VA

Note: The relays are energised when the system is in a 'healthy' state, and will 'relax' to their normally open condition if the mains power input is disconnected, or the 'Reset' condition is applied, thereby automatically signalling a fault condition.

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1.4.1 The following will be detected and signalled as an **Alarm** condition:

Failure to correct all incoming errors (more than 8 errored bytes per MPEG frame).*

1.4.2 The following will be detected and signalled as a **Fail** condition:

Loss of incoming clock transitions.
Loss or corruption of PSYNC or DVALID, or code 47H not coincident with PSYNC.*
Input data rate too high.
Hardware/firmware failure, failure to configure.
PSU failure or out of limits.

*These may be disabled by strapping options for the transport of non-MPEG data formats.

Note: All Alarm and Fail criteria are subject to a persistence check of 2-4 seconds.

1.5 Power Supply Input

1.5.1 Mains **In its mains-powered form, the unit is Class 1 equipment, and therefore requires an earth connection.** A single male filtered mains connector, approved to IEC 320, is provided on the rear panel, along with a seperate 20mm mains protection fuse holder approved to IEC 257. **A 20mm mains fuse of 2AT rating, approved to IEC 127 and UL recognised, must be used at all times.** The connector and fuse-holder are located at the far right of the panel when viewed from the rear. The integral mains power supply is autosensing/autoranging for operation at the following supply ratings: Single phase 50-60Hz, 100-240V(rms). Typical power consumtion is 20VA.

1.5.2 48VDC A 48 VDC power input option is also available, in which connection is made via a terminal strip on the rear panel. The unit is reverse polarity protected, and the correct polarity is marked adjacent to the connector. The fuse type is 2AF **quickblow.** The supply inputs are floating, so to guarantee ground continuity **it is strongly recommended that the chassis bonding stud is wired to an appropriate earth point on the equipment rack.** The recommended input voltage range is 40.5-57Volts DC. Typical power consumption is 20VA.

The chassis bonding stud is available adjacent to the power connector, and is internally connected to the chassis ground (Ov)

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1.6 Front Panel Status Indications

The ARG 1834 TX has two sets of LEDs on the front panel. Their function is as follows:

1.6.1 The left-hand bank, viewed from the front, indicate the following:

Alarm	:	Amber LED	
Fail	:	Red LED	**See section 1.4 for definition of Alarm and Fail conditions**
Power active	:	Green LED	

1.6.2 The right-hand bank, viewed from the front, indicate the currently active input, i.e. ASI (Copper), ASI (Optical) if fitted, or SPI (Parallel LVDS).

Input carrier present and selected (one only) : Green LED
(i.e. this indicates the currently active input)

Input carrier present but **not** selected : Amber LED
(another input must already be active)

See Section 1.1.3 for a description of the input priority system.

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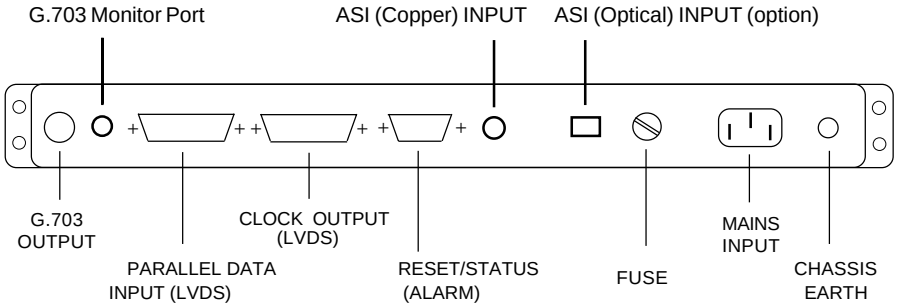
1.7 Physical Construction

The ARG 1834 TX unit is housed in a 19" Euro-rack enclosure of 1U height, and depth 390mm including connectors. LED status indicators are provided on the front panel, and connectors for the Telecom Network Interface and incoming data stream are located on the rear panel, along with an auxiliary connector for Alarm signalling. Use of the adjustable support kit (supplied with the unit) is recommended.

Each unit weighs approximately 5kg, the support kit 2kg (8.5kg in its packing for shipment)

Rear Panel View (ARG 1834 TX Mains powered version)

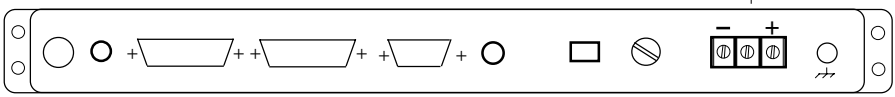


Notes:

a) An internal link option is available to convert this port into an SPI (LVDS) output port, when using an ASI Transport Stream input. (See Section 1.8)

b) For 48VDC powered versions, a terminal strip replaces the mains connector. Please observe the polarity as marked (centre terminal is not connected).

Rear Panel View (ARG 1834 TX - 48VDC powered version)



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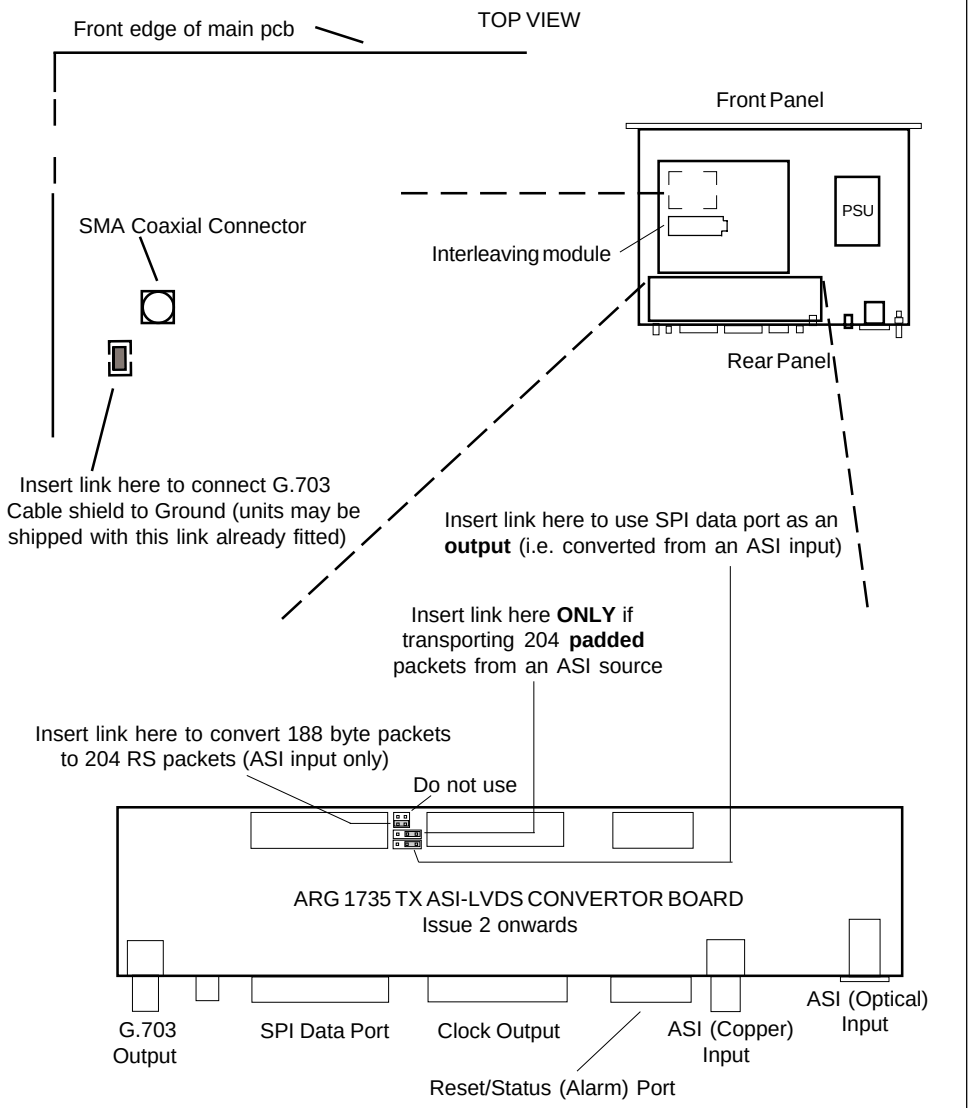
1.8 ARG1834 TX Link Settings (see also Section 1.9)


TOP VIEW
Front edge of main pcb
Front Panel
PSU
SMA Coaxial Connector
Interleaving module
Rear Panel
Insert link here to connect G.703 Cable shield to Ground (units may be shipped with this link already fitted)
Insert link here to use SPI data port as an **output** (i.e. converted from an ASI input)
Insert link here **ONLY** if transporting 204 **padded** packets from an ASI source
Insert link here to convert 188 byte packets to 204 RS packets (ASI input only)
Do not use
ARG 1735 TX ASI-LVDS CONVERTOR BOARD
Issue 2 onwards
G.703 Output
SPI Data Port
Clock Output
ASI (Copper) Input
ASI (Optical) Input
Reset/Status (Alarm) Port

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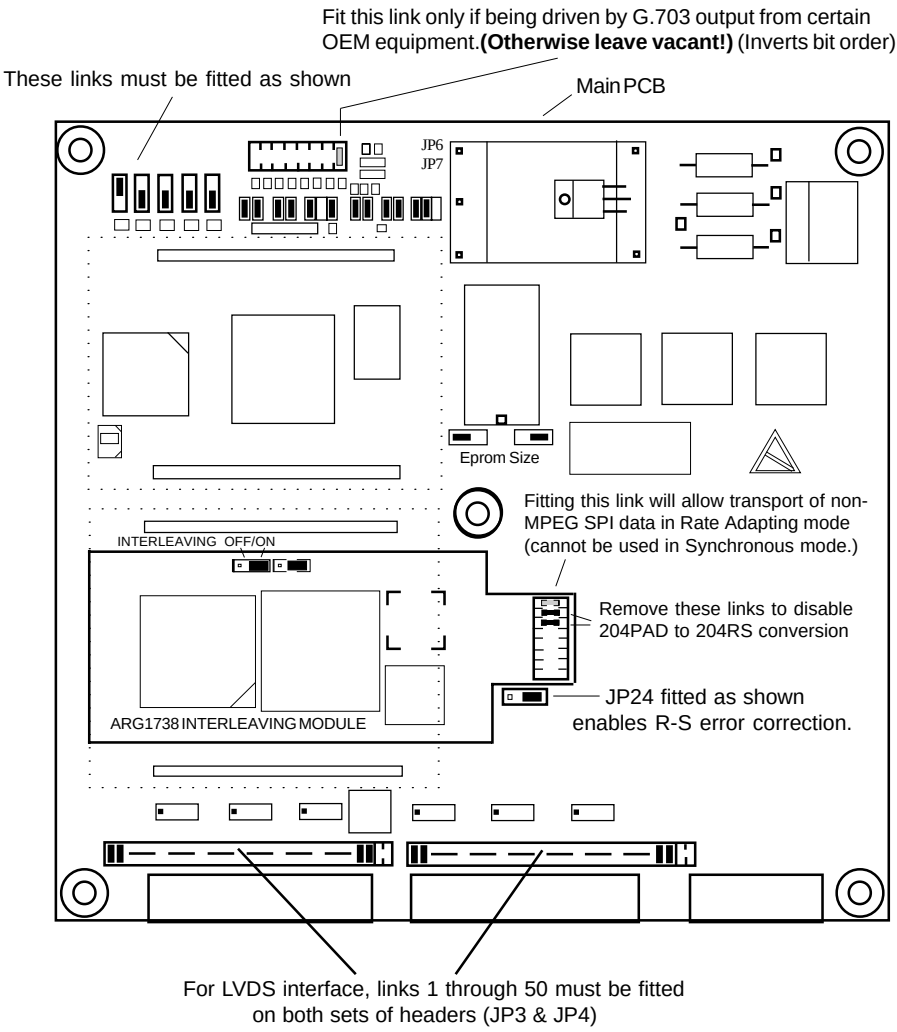
1.9 ARG1834 TX General Link Settings (see also Section 1.8)


Fit this link only if being driven by G.703 output from certain OEM equipment.**(Otherwise leave vacant!)** (Inverts bit order)
These links must be fitted as shown
Main PCB
JP6
JP7
Eprom Size
Fitting this link will allow transport of non-MPEG SPI data in Rate Adapting mode (cannot be used in Synchronous mode.)
INTERLEAVING OFF/ON
Remove these links to disable 204PAD to 204RS conversion
JP24 fitted as shown enables R-S error correction.
ARG1738 INTERLEAVING MODULE
For LVDS interface, links 1 through 50 must be fitted on both sets of headers (JP3 & JP4)

TITLE	DRAWN	CHECKED	APPROVED	DATE
ARG 1834 USER MANUAL	CRW	GF	CRW	20.4.98
	DRAWING NO: 1834-EQ001-PS16			

ISSUE	DESCRIPTION	APPD	DATE
3	ECN4156	MH	30.09.99
4	ECN4463	MH	10.01.01
5	ECN4479, ECN4514	SL	18.05.01

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2.0 ARG1834 RX SPECIFICATION

The ARG1834 RX unit terminates a 34.368Mb/s G.703 (E3) Telecom Network or Line, performs serial-to-parallel conversion, rate adaption, Reed-Solomon error checking and correcting if required, monitoring for fault or alarm conditions, and reformats the data into DVB Compliant Transport streams in both SPI and ASI formats. Assuming the received data is from a matching ARG1834 TX unit, the ARG1834 RX automatically detects the original input byte rate, packet type and ASI packet or byte space format if applicable, and reconstructs this from the incoming G.703 line signal. ('Transparent' Network-synchronised 34.368Mb/s parallel data may also be transported). To facilitate simple redundancy switching, duplicate data outputs are provided with separate drivers, etc.

Telecom Input Interface : E3 Interface at 34.368Mb/s, using HDB-3 line coding, compliant with ITU-T Recommendation G.703, unframed.

Input Connector : 75ohm BNC coaxial, isolated from chassis (earth link available)

Output Interfaces (2 off) : DVB ASI (Copper) interfaces as defined in EN 50083-9 and DVB-PI-232
and (2 off): DVB SPI (LVDS) interfaces as defined in EN 50083-9 and DVB-PI-232
and (2 off): DVB ASI (Optical) interfaces (- - - ditto- - -) - **Factory Option**

Output Connectors (2 off): 25 way female 'D' type connector with threaded locking posts (SPI)
and (2 off) : 75 ohm BNC coaxial (ASI Copper)
and (2 off) : SC type Multi-mode Fibre connectors (ASI Optical) **- Factory Option**

Output signal levels : LVDS (Low Voltage Differential Signalling) (SPI)
: 800mV p/p +/-10% (ASI Copper)
: -14 to -20 dBm (average) (ASI Optical)

Power Supply : Single-phase auto-sensing mains input, 100-240 Vrms a.c. 50-60 Hz.
or : 48 VDC (factory option) 40.5-57VDC range
Typical consumption : 25VA
Mains Input Fuse : 2AT (2 Amp Anti-Surge as per IEC 127) and UL recognised.

48 VDC Input Fuse : 2A 'quickblow' (2AF)

Auxiliary Control Signals : Summary alarm/fail indications, via Form 'C' relay contacts, with reset input

Auxiliary Connector : 9-way 'D' type female connector, with threaded locking posts

Operating Temperature : 0degC to +40degC

Storage Temperature : -5degC to +70degC
Safety : EN 60950 73/23/EEC (LVD Europe), UL 1950 listed 3rd edition, CSA 950-95

TITLE	DRAWN	CHECKED	APPROVED	DATE
ARG 1834 USER MANUAL	CRW	GF	CRW	20.4.98
	DRAWING NO: 1834-EQ001-PS17			

ISSUE	DESCRIPTION	APPD	DATE
3	ECN4156	MH	30.09.99
4	ECN4463	MH	10.01.01
5	ECN4479, ECN4514	SL	18.05.01

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EMC : EN 55022; EN 50082-1, 89/336/EEC (Europe)
47CFR CH.1 (FCC) Part 15. Subpart B, Class A

Link Options **(Refer to sections 2.7 and 2.8 for link locations)**

: FEC on/off (factory default = on)	(see section 2.2)
: De-Interleaving on/off (factory default = on)	(see section 2.2)
: G.703 line equalisation	(see section 2.1)
: Disable automatic 204RS to 188 byte conversion (only converts if original input was 188 byte)	(see section 2.2.5)
: G.703 B.E.R. alarm sensitivity	(see section 2.3.1)
: MPEG Packet auto configuration	(see section 2.2)
: Bit order inversion (for compatibility with certain OEM equipment)	(see section 2.1)
: Forcing of ASI space format (byte or packet)	(see section 2.2.4)
: Use of SPI port as an input (for LVDS to ASI conversion)	(see section 2.2.1)
: Transmission of non-MPEG SPI data (not in Synchronous mode)	(see section 2.3.2)

Factory Options : ASI Optical outputs, 48VDC power input
: Contact factory for T1, E1, E2, DS-3, E4, STM-1 variants

2.1 Telecom Network Input Interface

The ARG 1834 RX unit is designed to accept a standard unframed 34.368Mb/s (E3), HDB-3 encoded data stream as per ITU-T Recommendation G.703 for Physical/Electrical characteristics of hierarchical digital interfaces.

Connection to the Telecom Network is transformer-coupled through a 75 ohm BNC coaxial socket mounted on the rear panel.

Note: There are 4 different link-selectable options to set the most appropriate line equalisation characteristics. These are set at manufacture to the most common settings, but may be changed if unusual line conditions are encountered. (see Section 2.7)

There is also a link setting which will enable the unit to correctly receive the G.703 signal generated by some other OEM equipment, by reversing the bit order. (Synchronous mode only - see Section 2.8).

As the line data will in most cases have been generated by a matching ARG1834 TX unit, the ARG1834 RX unit will be able to determine the original data byte rate, and reconstruct the original byte rate and packet type from the incoming G.703 line signal. Alternatively, the units may also be used in 'transparent' mode in which a 34.368Mb/s data stream may be transported across the Telecom Network, synchronised at the Transmit end to a 4.296MHz byte rate clock derived from the Network clock.

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2.2 Output Interfaces

The ARG1834 RX unit provides dual DVB ASI and dual DVB SPI outputs to drive subsequent equipment and allow for redundancy switching. Each output has its own drivers, and each output transmits the same data, conforming to EN 50083-9 and to DVB-PI-232, i.e. 8 bit parallel data + clock, etc for the SPI outputs, and serial 270Mb/s data for the ASI outputs.

In normal use, the outgoing data streams faithfully reproduce the original data stream, so MPEG-2 data will be in one of three formats:

a) packets of 188 data bytes
b) packets of 188 data bytes plus 16 padding bytes
c) packets of 188 data bytes plus 16 Reed-Solomon check bytes

Packet recognition and reconstruction is usually automatic, but link options are also provided, **and are in fact recommended if using Synchronous mode.** (see Section 2.7)

(i) In it's default setting when shipped,'Embedded Auto Format', the ARG1834 RX unit receives information in the data stream which instructs it to process the incoming data into one of the above formats.

(ii) In 'Local Auto Format' mode, the unit checks for Reed-Solomon functionality within the incoming data stream, and also monitors the MPEG frame length, and thereby determines the correct data structure to be reapplied.

(iii) In 'Local Manual' mode, links can be set to force the unit to format the data into one of the above three formats.

Once the incoming information has been converted into byte-wise parallel data, the Reed-Solomon check bytes, if present, will be used to correct any corrupted data, if possible. If the errors are not recoverable, the error flag in the packet header will be set to '1' and the data will be left unchanged. The Reed-Solomon check bytes will be recalculated to protect the 'new' data. The ARG1834 RX unit cannot reset the error flag if already set to '1' within the incoming data stream. If there are no received errors, or the received errors are recoverable, the recalculated Reed-Solomon check bytes are forwarded on to protect the integrity of the data over the next link in the transmission path

There is a link option to disable Reed-Solomon operation if desired (see section 2.8, link JP7)

DVB - compliant De-Interleaving (depth 12) (set as default) may be used to recover data from a suitably Interleaved source. (see section 2.8)

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2.2.1 The DVB SPI outputs are available in LVDS form, and are accessed via 25 way female 'D' type connectors on the rear panel, as shown below. **Data changes on the falling edge of the clock on pin 1.**

Pin		Signal	Pin		Signal
1	:	Clock A	14	:	Clock B
2	:	System Gnd	15	:	System Gnd
3	:	Data 7 A (MSB)	16	:	Data 7 B (MSB)
4	:	Data 6 A	17	:	Data 6 B
5	:	Data 5 A	18	:	Data 5 B
6	:	Data 4 A	19	:	Data 4 B
7	:	Data 3 A	20	:	Data 3 B
8	:	Data 2 A	21	:	Data 2 B
9	:	Data 1 A	22	:	Data 1 B
10	:	Data 0 A	23	:	Data 0 B
11	:	DValid A	24	:	DValid B
12	:	PSync A	25	:	PSync B
13	:	Cable Shield			

Note that there is a link option to use one LVDS port (B) as an INPUT (see Section 2.7)

2.2.2 The DVB ASI (Copper) outputs are accessed via 75 ohm BNC coaxial connectors on the rear panel. (see Section 2.6)

2.2.3 The DVB ASI (Optical) outputs, where fitted (Factory option), are accessed via SC style optical connectors on the rear panel. (see Section 2.6)

2.2.4 By default, the ASI outputs will have the same space format as the original Transport Stream input. It is, however, possible to force the output to either byte or packet space by fitting a link and removing a jumper cable, as shown in Section 2.7. If the original stream was in SPI format, the ASI outputs will be packet spaced by default.

2.2.5 It is also possible to automatically convert 204RS streams to 188 byte ASI streams (only if original stream started off as 188 byte, converted to 204RS format by an ARG1834TX). A link normally disables this facility (see section 2.7)

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2.3 Auxiliary Interface

The ARG18140 RX unit provides the following alarm/fail/reset functionality via a 9-way filtered 'D' type female connector mounted on the rear panel.

Pin connections:

Pin		Signal
Pin 1	:	Protective ground
Pin 2	:	Fail relay (Common)
Pin 3	:	Alarm relay (Normally Open in Alarm condition)
Pin 4	:	Alarm relay (Normally Closed in Alarm condition)
Pin 5	:	Reset input 1
Pin 6	:	Fail relay (Normally Open in Fail condition)
Pin 7	:	Fail relay (Normally Closed in Fail condition)
Pin 8	:	Alarm relay (Common)
Pin 9	:	Reset input 2
Relay type	:	BT Type 53, 1A switch rating 125V dc/ac, 30VA

Note: The relays are energised while the system is in a 'healthy' state, and will 'relax' to their normally open condition if the mains power input is disconnected, or the 'Reset' condition is applied, thereby automatically signalling a fault condition.

2.3.1 The following will be detected and signalled as an **Alarm** condition:

2.3.1.1 Failure to correct 3 consecutive MPEG frames (i.e. frames with more than 8 errored bytes) *

In addition, if a link is removed internally (see section 2.7 on Link Settings), the following will also signal an **Alarm**:

2.3.1.2 Received line error rate >1 in 10^6

2.3.1.3 Failure to correct all incoming errors in a ***single*** frame (more than 8 errored bytes per single MPEG frame).*

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2.3.2 The following will be detected and signalled as a **Fail** condition:

2.3.2.1 Loss of HDB-3 line signal.

2.3.2.2 Loss of proprietary framing.

2.3.2.3 Loss of MPEG framing (47H monitor).*

2.3.2.4 PSU failure or out-of-limits.

2.3.2.5 Hardware/firmware failure.

2.3.2.6 Loss of payload.*

Notes: **a)** All Alarm and Fail criteria are subject to a persistence check of 2 to 4 seconds.
b) *These functions may be disabled by internal strapping options for the transport of non-MPEG data formats.

The ARG1834 RX unit may be reset by the application of a short circuit between pins 5 and 9 on the Auxiliary Connector. While this condition is applied and held, the ARG1834 RX unit will be held in a reset state in which it will not respond to the incoming G.703 (E3) stream from the Telecoms Network/Line System. Both the Alarm and Fail relays will be de-activated, signalling an Alarm/Fail condition to appropriately connected equipment. Internally stored alarm/fail states, and any other internally stored status information, will be erased.

Upon removal of the short circuit, the ARG1834 RX unit will go through a re-start sequence in which major circuit functions will be re-initialised. There will be a finite delay before the unit will re-commence monitoring the incoming Telecom data stream and performing its synchronisation and data rate conversion tasks.

2.4 Power Supply Input

2.4.1 Mains **In its mains-powered form, the unit is Class 1 equipment, and therefore requires an earth connection.** A single male filtered mains connector, approved to IEC320, is provided on the rear panel, along with a seperate 20mm mains protection fuse holder approved to IEC 257. **A 20mm mains fuse of 2AT rating, approved to IEC 127 and UL recognised, must be used at all times.** The connector and fuse-holder are located at the far right of the panel when viewed from the rear. The integral mains power supply is autosensing/autoranging for operation at the following supply ratings : Single Phase 50-60Hz, 100-240V(rms). Typical power consumption is 20VA.

2.4.2 48VDC A 48 VDC power input option is also available, in which connection is made via a terminal strip on the rear panel. The unit is reverse polarity protected, and the correct polarity is marked adjacent to the connector. The fuse type is 2AF **quickblow.** The supply inputs are floating, so to guarantee ground continuity **it is strongly recommended that the chassis bonding stud is wired to an appropriate earth point on the equipment rack.** The recommended input voltage range is 40.5-57Volts DC. Typical power consumption is 20VA.

The chassis bonding stud is available adjacent to the power connector, and is internally connected to the chassis ground (Ov).

2.5 Status Indication

The ARG1834 RX unit has the following LED indicators on the front panel:

Fail : Red LED

Alarm : Amber LED

Power Active : Green LED

See Section 2.3 for definition of Alarm Fail conditions.

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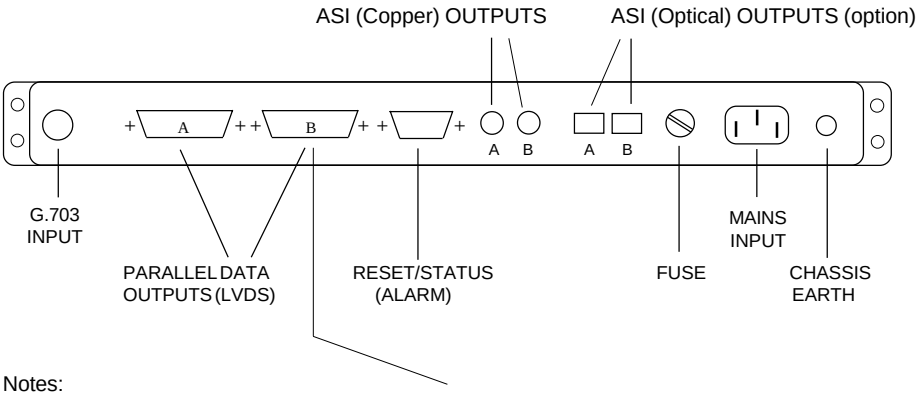
2.6 Physical Construction

The ARG1834 RX unit is housed in a 19" Euro-rack enclosure of 1U height, and of depth 390mm including connectors. LED status indicators are provided on the front panel, and connectors for the Telecom Network input and data outputs are located on the rear panel, along with an auxiliary connector for alarm signalling. Use of the adjustable support kit (supplied with the unit) is recommended

Each unit weighs approximately 5kg, the support kit 2kg (8.5kg in its packing for shipment)

Rear Panel View (ARG 1834 RX-Mains powered)

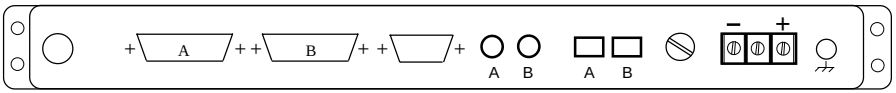


Notes:

a) An internal link option is available to convert this port (B) into an SPI (LVDS) **input** port, in which case the ARG 1834 RX unit can be used as an LVDS to ASI convertor. (See Section 2.7)

b) For the 48 VDC powered version, the IEC mains connector is replaced with a simple barrier strip termination, with the polarity clearly marked on the rear panel. **It is recommended that the chassis earth stud is connected to a suitable rack earth during installation, as the 48VDC inputs are isolated from the chassis. Note also that a 2A(F) 'quickblow' fuse is recommended for the 48 VDC units.**

Rear Panel View (ARG1834RX - 48VDC powered version)



TITLE	DRAWN	CHECKED	APPROVED	DATE
ARG 1834 USER MANUAL	CRW	GF	CRW	20.4.98
	DRAWING NO: 1834-EQ001-PS24			

ISSUE	DESCRIPTION	APPD	DATE
3	ECN4156	MH	30.09.99
4	ECN4463	MH	10.01.01
5	ECN4479, ECN4514	SL	18.05.01

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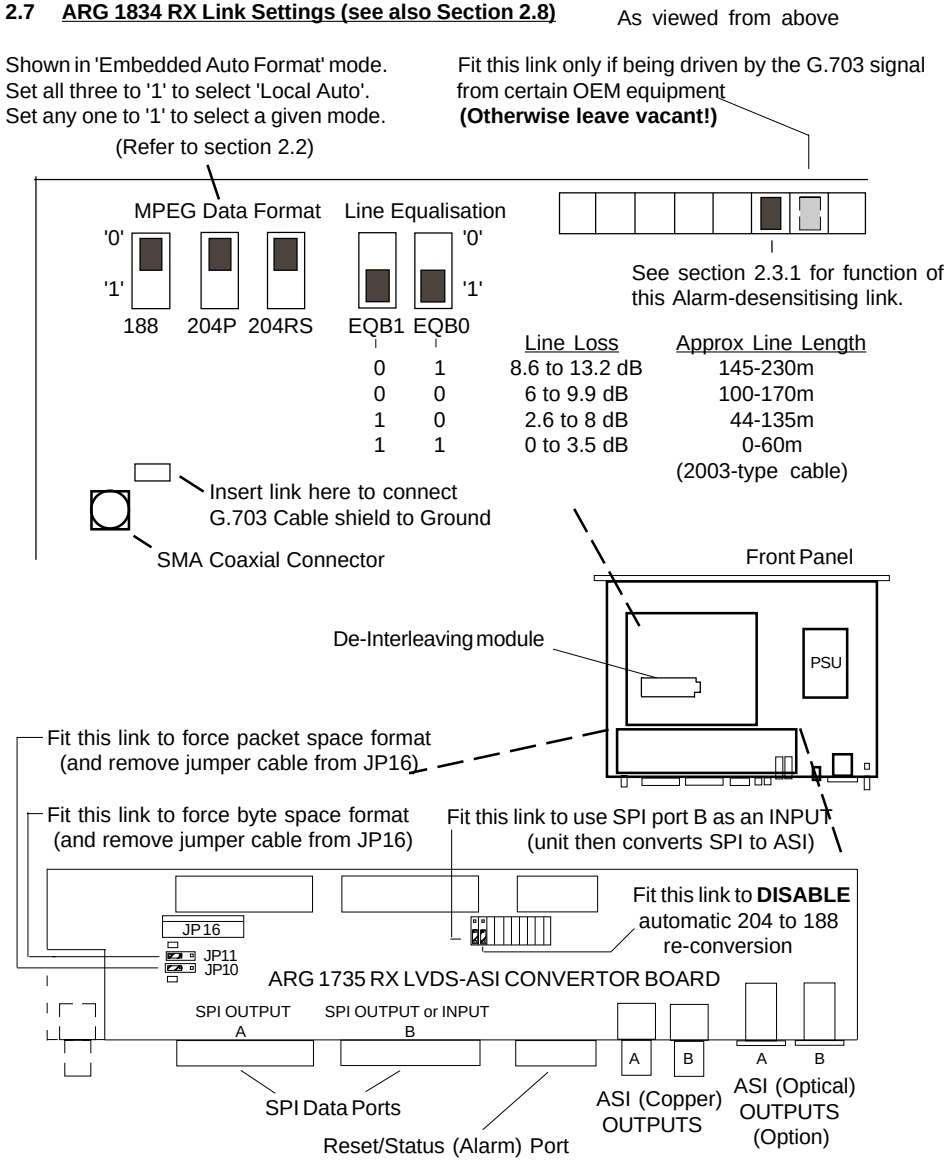
2.7 ARG 1834 RX Link Settings (see also Section 2.8)


As viewed from above
Shown in 'Embedded Auto Format' mode.
Set all three to '1' to select 'Local Auto'.
Set any one to '1' to select a given mode.
(Refer to section 2.2)
Fit this link only if being driven by the G.703 signal from certain OEM equipment
(Otherwise leave vacant!)
MPEG Data Format
Line Equalisation
'0'
'1'
188
204P
204RS
EQB1
EQB0
See section 2.3.1 for function of this Alarm-desensitising link.
Line Loss
Approx Line Length
0 1 8.6 to 13.2 dB 145-230m
0 0 6 to 9.9 dB 100-170m
1 0 2.6 to 8 dB 44-135m
1 1 0 to 3.5 dB 0-60m
(2003-type cable)
Insert link here to connect G.703 Cable shield to Ground
SMA Coaxial Connector
Front Panel
De-Interleaving module
PSU
Fit this link to force packet space format (and remove jumper cable from JP16)
Fit this link to force byte space format (and remove jumper cable from JP16)
Fit this link to use SPI port B as an INPUT (unit then converts SPI to ASI)
Fit this link to DISABLE automatic 204 to 188 re-conversion
JP16
JP11
JP10
ARG 1735 RX LVDS-ASI CONVERTOR BOARD
SPI OUTPUT A
SPI OUTPUT or INPUT B
A
B
A
B
SPI Data Ports
Reset/Status (Alarm) Port
ASI (Copper) OUTPUTS
ASI (Optical) OUTPUTS (Option)

TITLE	DRAWN	CHECKED	APPROVED	DATE
ARG 1834 USER MANUAL	CRW	GF	CRW	20.4.98
	DRAWING NO: 1834-EQ001-PS25			

ISSUE	DESCRIPTION	APPD	DATE
3	ECN4156	MH	30.09.99
4	ECN4463	MH	10.01.01
5	ECN4479, ECN4514	SL	18.05.01

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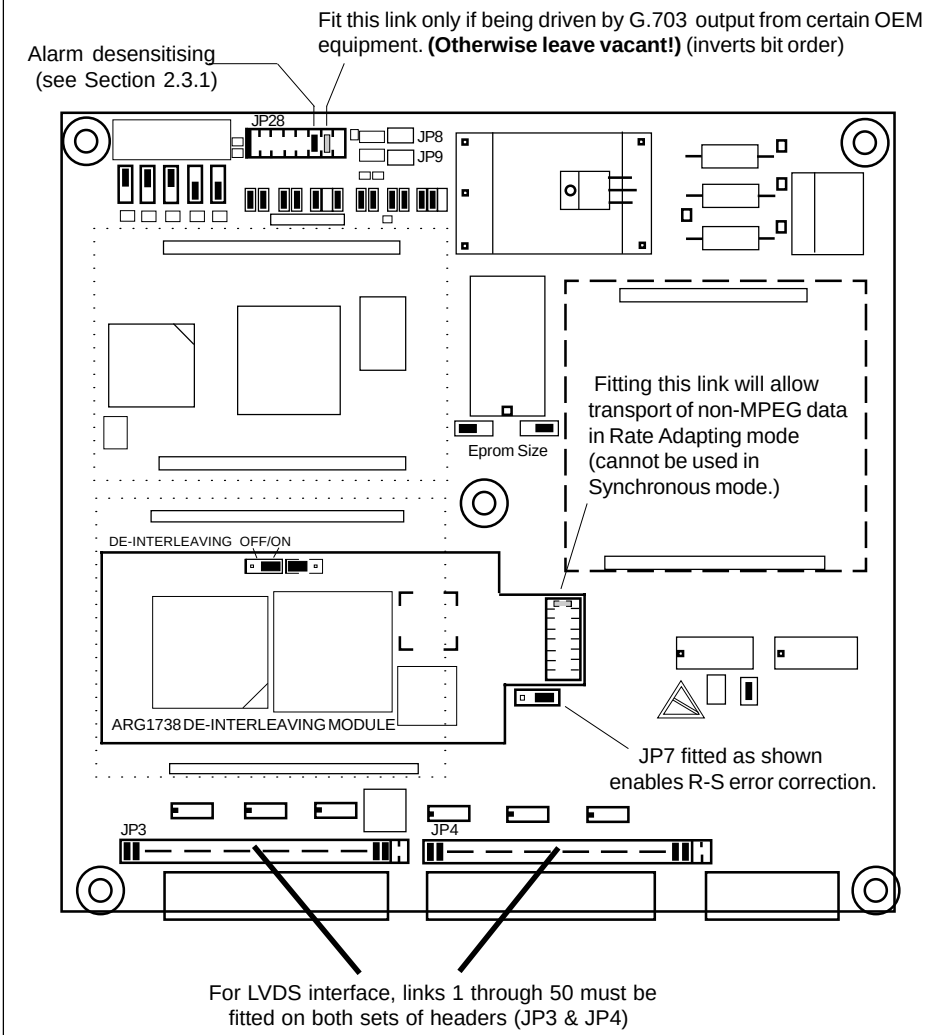
2.8 ARG1834 RX General Link Settings (see also Section 2.7)


Fit this link only if being driven by G.703 output from certain OEM equipment. **(Otherwise leave vacant!)** (inverts bit order)
Alarm desensitising (see Section 2.3.1)
JP28
JP8
JP9
Eprom Size
Fitting this link will allow transport of non-MPEG data in Rate Adapting mode (cannot be used in Synchronous mode.)
DE-INTERLEAVING OFF/ON
ARG1738 DE-INTERLEAVING MODULE
JP7 fitted as shown enables R-S error correction.
JP3
JP4
For LVDS interface, links 1 through 50 must be fitted on both sets of headers (JP3 & JP4)

TITLE	DRAWN	CHECKED	APPROVED	DATE
ARG 1834 USER MANUAL	CRW	GF	CRW	20.4.98
	DRAWING NO: 1834-EQ001-PS26			

ISSUE	DESCRIPTION	APPD	DATE
3	ECN4156	MH	30.09.99
4	ECN4463	MH	10.01.01
5	ECN4479, ECN4514	SL	18.05.01

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